كلية التقنية الالكترونية
College of Electronic Technology - Tripoli

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رقم القيد ..... اسم الطالب :.....

Total number of questions: 11 in 5 pages.. No of questions to be answered:11....

Q1-Put (✓) for right answer and (×) for wrong answer (5x0.5=2.5marks)

1-1. in MIPS systems pipelining hazards are avoided by hardware
1-2. supercomputers are used for high speed real time applications such as forecasting
1-3. computer networking is a kind of distributed computing
1-4. cache level size increase as that level closer to CPU
1-5. cache level speed increase as that level closer to CPU

Q2-Fill the following table by the corresponding statements number from 1 to 6 (6*0.5=3marks)

Computer Architecture	Computer Organization

1. involves Logic (Instruction sets, Addressing modes, Data types)
2. is concerned with the way hardware components are connected together to form a computer system.
3. is concerned with the structure and behavior of a computer system as seen by the user.
4. helps us to understand the functionalities of a system.
5. involves Physical Components (Circuit design, Adders, MUX, Peripherals)
6. tells us how exactly all the units in the system are arranged and interconnected.

Q3- Choose the right answer (12x0.5 =6 marks)

3-1. in MIPS
- 23 23-bit registers, r0 = 1 always
- only MOV instructions access memory
- 23-bit instructions, variable size opcode
- all ALU operations are 3 address register operations
- all
- non of all

3-2. MIPS design is
- A stack architecture
- A general purpose register(GPRs) architecture
- An accumulator architecture
- all
- non of all

3-3. ISAs are distinguished according to their
- bits per instruction
- types, size, location and number of operands
- addressing modes
- all
- non of all

3-4. MIPS is
- has fixed instruction length
- a GPRs design
- RISC
- load/store memory access
- all
- non of all

3-5. in MIPS, Program counter is incremented automatically
- after finishing the execution of current instruction
- before finishing the execution of the current instruction
- after fetching of the current instruction
- after decoding of the current instruction
- before encoding of the current instruction
- before fetching of the current instruction

3-6. Instruction pipelining systems introduce
- faster single instruction execution-
- faster over all process execution
- faster hardware access
- faster program counter
- all
- none of all

3-7. in processors support pipelining, instructions are
- totally overlapped
- partially overlapped
- not overlapped
- fully paralleled

3-8. MIPS makes control unit design easier because
- Instructions are of same size
- Source registers always in same place
- Immediate same size
- Operations always on registers/immediates
- all
- not of all

3-9. in MIPS Program counter is incremented
- manually by any code user
- manually by code programmer
- automatically regarding the code
- all
- non of all

3-10. for cache memory system the best cache and code design is

- to increase cache misses probabilities
- to decrease cache hits probabilities
- to increase cache hits probabilities
- to decrease cache misses probabilities

3-11. A given application written in Java runs 12 seconds on a desktop processor. A new Java compiler is released that requires only 0.6 as many instructions as the old compiler. Unfortunately, it increases the cycle per instruction CPI by 1.1. How fast can we expect the application to run using this new compiler? :choose 1

- 1.2x0.6/12=0.06s
- 12x0 6/1.2=6s
- 12x0.6 x1.2=8.64s
- 12x1.2/0.6=24s

3-12. the most efficient parallel processing schema is

- SISD
- MIMD
- MISD
- SIMD

Q4-Answer the following (a to d) **(total = 10.5 marks)**

(a) what are the following abbreviations meaning **(5x0.5=2.5marks)**

- MIPS
- ISA
- RISC
- CISC
- MIMD

(b) what MIPS means? and what is the main specifications of MIPS (just fill the table)**(0.5*6=3marks)**

Registers number and sizes	
Memory access instructions	
Instruction size	
Opcode field size	
Maximum number of operands	

(c) regarding the use of cache memory, **tot=3mrks** [ii)(0.5*3 = 1.5marks) + ii)(3*0.5=1.5marks)]

(i) what is write through and write back mean? which gives faster overall process in case of huge data transfer

(ii) what is cache miss and cache hit? if the probability of cache hit is 95% what the probability of cache miss?

d) show by a sketch the memory (storage) hierarchy (from hard disk to CPU registers) showing the speed and size changes directions **(2marks)**

Q5-answer the following **(Total = 5marks)**

a) Sort properly the contents of the table below, just fill numbers starting from 1 to 6 **(6*0.5=3marks)**

Operating system	
Logic circuits	
Memory +registers + ALU+ control blocks	
Transistors and wires	
Programming language compiler	
Application	

b) using the table above list the items represent a hardware and software stating and showing the interface in between, **(1.5marks)**

c) give a proper name for the table figure **(0.5mark)**

Q6 answer the following **(Total = 10.5marks)**

1- state the pipelining hazards, **(1.5marks)**

2

2- Assume that a CPU uses instructions pipelining for 3 instructions, each instruction segmented to3 stages as

1. Fetch (F)
2. Decode (D
3. Execute (E)

By assuming that each stage takes **0.5** Clock Cycle(CC), 1CC = **3ns**, latency = 0 and all instructions are completely independent (no hazards) , do the following:

a)use sketching to show pipelining mechanism) **(1mark)**

b) calculate the time needed to finish the overall process of execution of the **3** instructions using

(i) sequential **(0.5 marks)**

(ii) pipelining **(0.5 marks)**

c) calculate the process throughput (instruction/s) in both cases, sequential and pipelining - **(2*0.5=1 mark)**

d) using your results calculate the speedup in this process. **(1 mark)**

e) again, under the same assumptions stated above

(i) calculate the time of *100* sequential instruction of 5 stages **(1 mark)**

(ii) if the time needed to finish a process of n instructions each of k stages is (k+(n-1)CC, calculate the time needed to finish a process of 100 pipelined instructions each of 5 stages **(1 mark)**

(iii) using your results from (i) and (ii) calculate the speedup **(1 mark)**

f)observing the speedup up factors in the two cases above (d and e(iii)), what you realize as larger number of instructions are pipelined? **(1mark)**

g) if we assume that instruction pipelining hazards and latency together cause a delay of 1 ns per 100 instructions in average, what is the time needed to finish a pipelined process of 1000 instructions (1mark)

Q7-Answer the following **(Total = 5.5marks)**

a)state the MIPS instructions types (formats), showing the bandwidth (in bits) and name of each field for each type

b)What is the type of the following MIPS instructions (just fill it in the following table 1) **(6*0.25=1.5 marks)**

Table 1. Some of MIPS instructions encoding

Instruction	format (type)	Op (hex)	rs	rt	rd	shmt	funct hex)	Address(offset)
ADD		0	reg	reg	reg	0	20	n.a
SUB		0	reg	reg	reg	0	22	n.a
LW		23	reg	reg	n.a	n.a	n.a	Address
SW		2B	reg	reg	n.a	n.a	n.a	Address
BEQ		4	reg	reg	n.a	n.a	n.a	Address
AND		0	reg	reg	reg	0	24	n.a
J		2	n.a	n.a	n.a	n.a	n.a	Address

reg=0 for r0, reg=1 for reg 1 and so on, rs=register source, rt= register target, rd =register destination (reg numbers are in decimal)

c) regarding the assembly MIPS code below, If we assume that we place the **Loop** label starting at location 80000 in memory and **Exit** label at end of this code, what is the MIPS machine code for this MIPs assembly code? just fill table 2

```
Loop:  add r5, r4, r3        ; r5=r4+r3
       add r6, r7, r5        ; r6=r7+r5
       LW r2, 2(r3)          ; r5= data at memory location addressed by (r3+2)
       beq r3, r2, Exit      ; if r3=r4 go to the code line addressed by label Exit (offset)
       j  Loop               ; go to loop
Exit:
```

Table 2 machine code

s/n	Memory location	Instruction code in assembly	Instruction code in hexadecimal and binary		Instruction size in bis
1	8000	add r5, r4, r3	Hex	0 5 4 3 0 20	32
			Bin	000000 00101 00100 00011 00000 010000	
2			Hex		
			Bin		
3			Hex		
			Bin		
4			Hex		
			Bin		
5			Hex		
			Bin		

c) regarding the flow of information choose the right order of the execution steps of only 1 of the following instructions (just put the right order numbers as 1,2,3.etc in front of each line below)

add r1,r2,r3
add instruction is operating in 4 steps

- The result from the ALU is written into the register file using bits 15:11 of the instruction to select the destination register (r1).

- Two registers, r2 and r3, are read from the register file; also, the main control unit computes the setting of the control lines during this step.
- The ALU operates on the data read from the register file, using the function code (bits 5:0, which is the funct field, of the instruction) to generate the ALU function.
- The instruction is fetched, and the PC is incremented.

lw r1, offset(r2)
load instruction is operating in five steps

- An instruction is fetched from the instruction memory, and the PC is incremented.
- A register (r2) value is read from the register file.
- The ALU computes the sum of the value read from the register file and the sign-extended, lower 16 bits of the instruction (offset).
- The data from the memory unit is written into the register file; the register destination is given by bits 20:16 of the instruction (r1).
- The sum from the ALU is used as the address for the data memory.

beq r1, r2, offset
beq instruction is operating in 4 steps
- Two registers, r1 and r2, are read from the register file.
- An instruction is fetched from the instruction memory, and the PC is incremented.
- The Zero result from the ALU is used to decide which adder result to store into the PC.
- The ALU performs a subtract on the data values read from the register file. The value of PC + 4 is added to the sign-extended, lower 16 bits of the instruction (offset) shifted left by two; the result is the branch target address.

Q8- -Assume 0.2% of the runtime of a program is not parallelizable. This program is supposed to run on a supercomputer machine, which consists of many cores. Under the assumption that the program runs at the same speed on all of those cores, and there are no additional overheads, what is the speedup can be achieved using 10, 100, 1000, 10000, 100000 and 1000000 cores? depending on your results, comment on the relation between speedup and number of cores. **(Total =4 marks)**

Number of cores (n)	Speedup S(n)
10	
1000	
10000	
100000	
1000000	
10000000	

Amdahl's Law

Speedup (S) =1 / ((1-P)+P/N)

Q9-Answer the following **(Total =7marks)**

1- Program execution time is made up of 50% CPU time and 50% I/O time. Assuming that no overlap between CPU and I/O operations,

a) which is the better enhancement: **(3marks)**

i) Increasing the CPU speed by 200% or
ii)reducing I/O time by 50%?

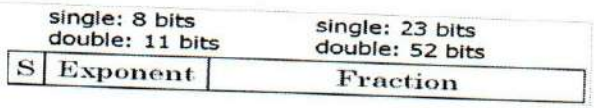
b)what is the maximum speedup as
i) CPU speed improved infinitely **(1mark)**
ii) IO speed improved infinitely **(1mark)**

Q10 referring to IEEE 754 floating point standard, answer the following **(Total =6.5 marks)**

a) (i) is this IEEE754 number**(11000000111000000000000000000000)** a single or double precision **(0.5mark)**
(ii) what decimal value of the above IEEE 754 number **(3marks)**

b)) what is the IEEE 754 value of the decimal number (-5) **(3marks)**

to convert IEEE 754 number to decimal use formula
$(-1)^s * (1 + f) * 2^{e\text{-bias}}$
s= sigh - e=exponent, f= fraction
here the s, f and e fields are assumed to be in decimal



Q11-answer the following **(Total = 6marks)**

a) state the main elements of data-path? what elements are represented in fig, 1 **(4marks)**
c) in MIPS how to select a register from register file? **(1mark)**
d) instruction decoding depends on which part of instruction 0.5mark
e) put the following processor design steps in right order (just put the right order numbers as 1,2,3.4,5 in front of each line below) 0.5*4=2marks

- Assemble the control logic
- . Analyze instruction set => datapath requirements
- Select set of datapath components & establish clock methodology
- Analyze implementation of each instruction to determine setting of control points that effects the register transfer.
- Assemble datapath meeting the requirements

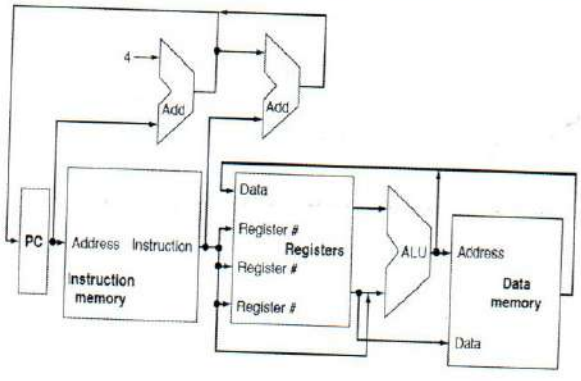


Fig 1

GOOD LUCK